Remarks

Reconsideration is respectfully requested.

Claims 1-22 were originally pending in this application.

Independent claims 1 and 11 are amended to more precisely claim the invention. Claim 1 is also amended to correct antecedent basis. Independent claim 23 is newly added. Claims 8 and 18 are amended to properly claim Markush groups.

In brief, the invention is specialized test software operating on an embedded processor that creates one or more test workers or threads, each having a specific routine to perform, which are executed in parallel, stressing various communication paths. The results may be analyzed to help in many different ways during the life cycle of a device containing the embedded processor.

The test software is a standardized test suite that is capable of exercising all of the input and output ports of an embedded processor, regardless if those input and output ports are used in a specific application. The test software may be preconfigured to exercise each of the input and output ports in various manners so that when powered up and operating, an engineer may diagnose and debug the circuitry of the device using standardized test software. The standardized test software may be reused for every board design or application that uses the embedded processor, and may greatly reduce the time required to 'turn on' a new circuit design.

The amended claims more distinctly point out some of the patentable features of the invention. The invention as claimed is a set of software routines developed for an embedded microprocessor. The software may be used when a new device is built using the embedded microprocessor and the software may exercise each input and output path of the microprocessor so that an engineer may debug the circuitry that makes up the input or output path.

35 USC §102(e) Rejections

Claims 1-21 are rejected under 35 USC 102(e) as being anticipated by DeRolf (US Pat 6,904,544).

The rejection is respectfully traversed for at least the following reasons.

The amendment to the independent claims 1 and 11 requires that the embedded processor "being operable on a single board having a fewer number of input ports than said embedded processor". DeRolf does not teach that the test software be used on a single board computer. DeRolf further does not teach that the embedded processor has more ports than is implemented on a single board and that the test software is capable of testing those unimplemented ports.

Part of the invention is to create a suite of software that is capable of testing an embedded processor in any application in which the processor may be used. Such a suite is created beforehand and tested to ensure that a full complement of test capabilities can be used when a new circuit board or component is initially debugged. An engineer can begin working on verifying the hardware design without having to debug test code simultaneously. This is in contract to DeRolf, where the test software is used after system installation. DeRolf does not recognize the complexities of turning on a new circuit design that are solved by this invention.

It is well-established law that, for a proper rejection of a claim under 35 U.S.C. § 103 (or 35 U.S.C. § 102) as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all elements, features, or steps of the claim at issue. See, e.g., *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). *Glaverbel S.A. v. Northlake Mkt'g & Supp., Inc.*, 45 F.3d 1550, 33 USPQ 2d 1496 (Fed. Cir. 1995) ("the claimed process, including *each step* thereof, *must have been described* or embodied, either *expressly or inherently*.") (Emphasis added.) As clearly articulated in M.P.E.P. § 2143.03, "[to] establish *prima facie* obviousness of a claimed invention, *all the claim limitations must be taught or suggested* by the prior art." *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). "*All words* in a claim *must be considered in judging the patentability* of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (C.C.P.A. 1970). (Emphasis added.)

DeRolf does not teach of timestamping an outgoing message or an incoming message as in claim 1. The Office cites Col 11:45-55 of DeRolf. DeRolf discloses a timestamp only for starting a record when the expert diagnostic tool is invoked.

The timestamp as disclosed in the specification is used to perform various analyses of data throughput and thus is one mechanism for measuring performance. An example is illustrated on page 13, line 29 of the specification: "By timestamping the outgoing and incoming messages, the amount of time for the message to travel can be computed. This information is useful in evaluating the amount of data that can be transmitted across an interface circuit. "

The claimed invention requires that an analysis routine analyze the outgoing and incoming messages. The Office cites DeRolf at Col 11:45-60. The analysis routine as described on the specification may analyze the timestamps to determine the length of time between messages and generate various statistics. Examples of such analyses are given in the Markush group of dependent claim 8.

Regarding independent claim 21, several claimed elements have not been discussed or cited by the Office. The Office has a duty to present a *prima facie* case of obviousness by citing each and every element of the claim. As discussed above, "the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all elements, features, or steps of the claim at issue."

Specifically, the Office has not cited with specificity where in the cited references are "a first command interpreter...adapted to operate on a first embedded processor" and "a second command interpreter...adapted to operate on a second embedded processor" are disclosed. The claims require that both the first and second processors are adapted to operate the "reusable test sequence" as claimed.

Applicant respectfully requests that the Office describe with specificity where in the prior art these limitations are shown in the cited art.

Applicant respectfully requests that the Office afford the Applicant an opportunity to respond and thus requests that if the Office uphold the rejection, that such rejection be done in a non-final Office action.

Regarding claims 6 and 16, the Office rejects the claims citing DeRolf at Col 3:59-67. The claims require multiple threads of commands. A thread is a computer science construct. From http://en.wikipedia.org/wiki/Thread_(computer_science), viewed 12 Feb 2008:

> A thread in computer science is short for a thread of execution. Threads are a way for a program to fork (or split) itself into two or more simultaneously (or pseudo-simultaneously) running tasks. Threads and processes differ from one operating system to another but, in general, a thread is contained inside a process and different threads of the same process share some resources while different processes do not.

DeRolf makes no mention of threads, threading, processes, or any type of similar low level programming constructs.

Regarding claims 7 and 17, the Office rejects the claims citing DeRolf at Col 13:15-20. The claims require validation of an incoming message. Validation may be performed, for example, by transmitting a message through a communications loop and comparing the outgoing message with the incoming message. In this manner, validation can identify problems with a communication circuit.

In the cited passage, DeRolf describes:

> determining a path in the system to test, wherein the path includes path components including at least a host adaptor, a link, a device interface, and a device, wherein the device comprises a storage system;
>
> performing an initial test to determine if there is a failure in the path;

Validation is a very specific method for testing a communication path, and is not described in DeRolf.

Regarding claims 8 and 18, the Office rejects the claims citing DeRolf at Col 4:13-20. Claims 8 and 18 are amended to properly claim Markush groups. The claims require several different specific analyses that may be performed on message paths. These analyses include

"message transfer time, average message transfer time, and average data throughput per unit time". No such tests, statistics, or analyses are disclosed in DeRolf.

Regarding claims 9 and 19, the Office rejects the claims citing DeRolf at Col 13:15-20. The claims require an "initiator adapted to determine if an I/O device is present". DeRolf recites a "device interface", but a "device interface" is a passive thing. An "initiator" is an active thing that "determines if an I/O device is present". DeRolf does not teach that the "device interface" is anything but a passive component and does not teach that the "device interface" can perform any active functions, let alone "determining if an I/O device is present" as claimed.

Similarly, claims 10 and 20 are rejected citing DeRolf at Col 11:13-20. The claims require that the initiator be "further adapted to perform a diagnostic routine with said I/O device". In addition to the above arguments, the citation clearly states that "[t]o initiate the diagnostic routine at block 200 in Fig. 3, the administrator would specify a path..." (emphasis added). This teaches away from having an initiator as a component in a software diagnostics platform.

Independent claim 22 is rejected under 35 USC 102(e) citing Oberlaender (US PGPUB 2005/0102572). Applicant respectfully traverses the rejection for at least the following reasons.

Oberlaender does not describe "software operable on said embedded processor, said software adapted to enable said circuit to perform said predefined function". The Office cites Col 3:0023 "equivalency checking".

The reference to "equivalency checking" in paragraph 23 of Oberlaender is not "software operable on said embedded processor". From Oberlaender in paragraph 0023:

> After the verification process is completed, a synthesis tool 118 is then utilized to convert the high-level circuit model into a lower-level description including actual components (e.g., gates) and a netlist defining the various connections between the actual components. Equivalency checking is typically performed to verify that this lower-level description accurately reflects the verified high-level model. (Emphasis added)

Oberlaender's "equivalency checking" is merely a verification of the "synthesis tool" that generates a netlist. This is not "software operable on said embedded processor".

The Office cites Col 3:0025 as being equivalent to the claimed "loading said embedded processor with a test platform software". In paragraph 0025, Oberlaender described only a "simulation model 205" on which software is simulated. The simulation model is not an actual embedded processor, but may be a simulation of one.

The difference between a simulated processor and an actual embedded processor is great. Among other physical and operational differences, the simulated processor may be used to verify that circuitry and software performs as designed but cannot in any way be used to verify how a circuit is manufactured. On the other hand, the software in an actual embedded processor may be used for both design and manufacturing verification.

The Office cites Col 4:0027 "interface circuit" as being equivalent to "a command interface adapted to receiving commands and outputting results". The "interface circuit 222" of Oberlaender is an interface within a memory array 220 and passes information between memory cells 226, a simulated CPU 210, and a debugging tool 230. See Figure 2 of Oberlaender. Nowhere in Oberlaender is it taught that the "interface circuit 222" is capable of receiving commands and outputting results as claimed.

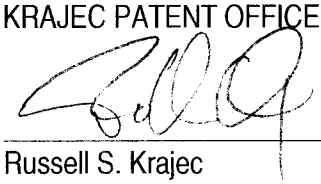
Applicant believes no new material has been added. Applicant invites the Examiner to call the undersigned at 970-690-4023 to suggest any changes or discuss any actions so that this case may be quickly allowed.

The applicant believes the application to be in condition for allowance, and such action is earnestly requested.

Dated this 15 day of Feb 2008 ~~2007~~.

Respectfully submitted:

KRAJEC PATENT OFFICES, LLC



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